

Chapter 3

FET Amplifiers

Spring 2012

4th Semester Mechatronics

SZABIST, Karachi

12 فوریاء 22

CH 3

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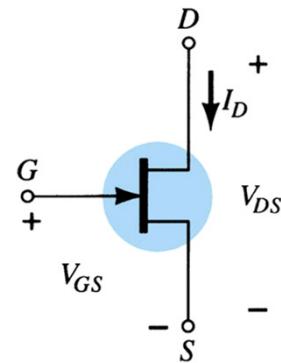
CH 3

- *JFET Small Signal Model*
- *Fixed Bias Configuration*
- *Self Bias Configuration*
- *Voltage Divider Configuration*
- *Common Gate Configuration*
- *Source Follower Configuration*
- *D and E type MOSFET Configurations*
- *FET Amplifier Network Design*
- *Cascade Configuration*
- *Applications*

FET *Small Signal Model*

FETs Advantages:

- Excellent voltage gain
- High input impedance
- Low-power consumption
- Good frequency range



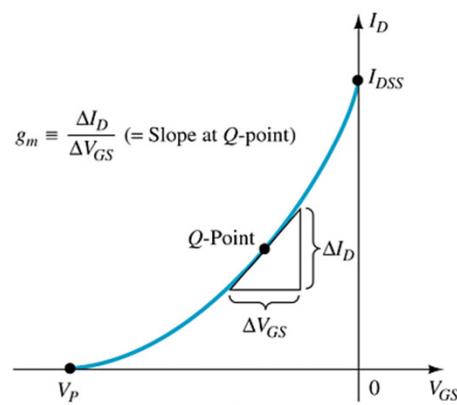
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Transconductance:

The relationship of a change in I_D to the corresponding change in V_{GS} :

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$



12، فروردین 22

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Mathematical Definition of g_m :

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Where $V_{GS} = 0V$

$$g_m = \frac{2I_{DSS}}{|V_P|} \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

Where

$$g_m = g_{m0} \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_P} \right)$$

12 . ٢٢

CH 3

Example 8-1:

Determine the magnitude of g_m for a JFET with $I_{DSS} = 8 \text{ mA}$ and $V_P = -4 \text{ V}$ at the following dc bias points:

- a. $V_{GS} = -0.5 \text{ V}$
- b. $V_{GS} = -1.5 \text{ V}$
- c. $V_{GS} = -2.5 \text{ V}$

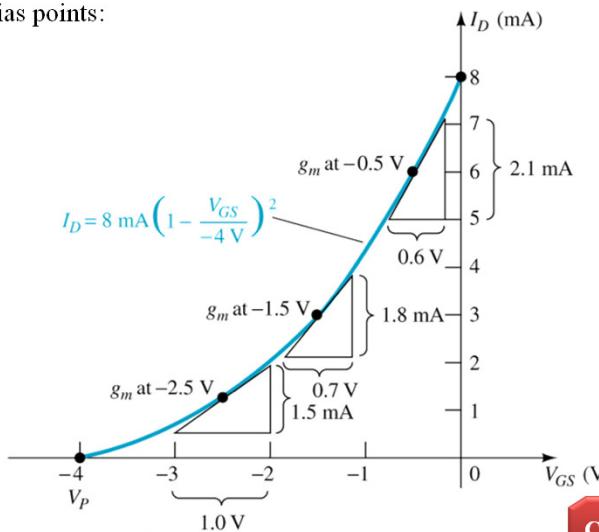
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FET
AmplifiersFET Small Signal Model ⁹**Example 8-1:**

Determine the magnitude of g_m for a JFET with $I_{DSS} = 8 \text{ mA}$ and $V_P = -4 \text{ V}$ at the following dc bias points:

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- $V_{GS} = -1.5 \text{ V}$
- $V_{GS} = -2.5 \text{ V}$



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FET
AmplifiersFET Small Signal Model ¹⁰**Example 8-2:**

For the JFET of Ex 8-1, find:

- g_m (max)
- g_m at each point of Ex 8-1

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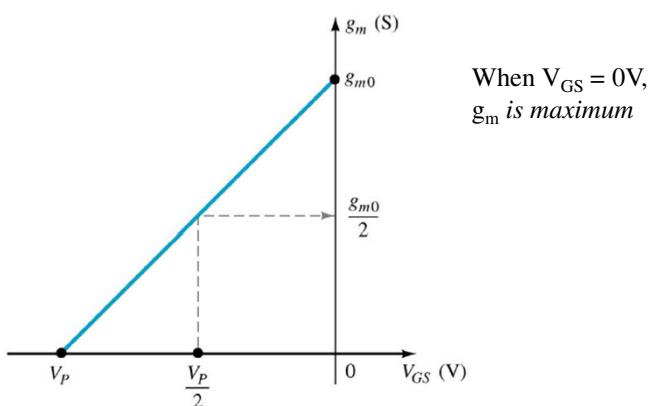
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FET Small Signal Model ¹¹

g_m vs V_{GS} :

When $V_{GS} = V_P$, g_m is zero



12 اسے 22

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FET Small Signal Model ¹²

Example 8-3:

Using JFET of Ex 8-1, plot g_m vs V_{GS} .

12 اسے 22

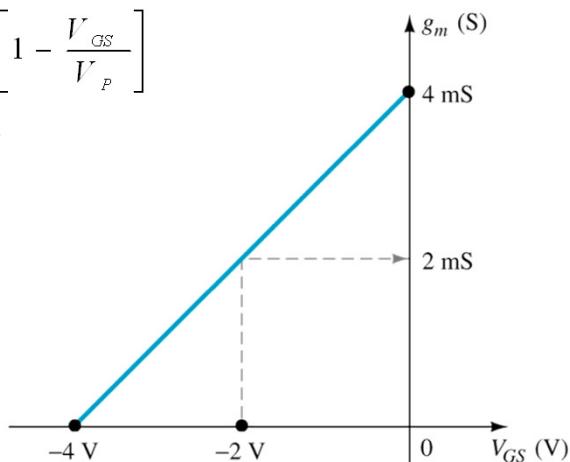
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**FET
Amplifiers**
FET Small Signal Model ¹³
Example 8-3:

Using JFET of Ex 8-1, plot g_m vs V_{GS} .

$$g_m = \frac{2 I_{DSS}}{|V_P|} \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$



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**FET
Amplifiers**
FET Small Signal Model ¹⁴
Effect of I_D on g_m :

Shockley's equation:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = g_{m0} \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

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FET Small Signal Model ¹⁵**Plot of I_D vs g_m :**

$$g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}} \quad g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$

g_m	I_D
g_{m0}	I_{DSS}
$0.707 g_{m0}$	$I_{DSS}/2$
$0.5 g_{m0}$	$I_{DSS}/4$
0	0 mA

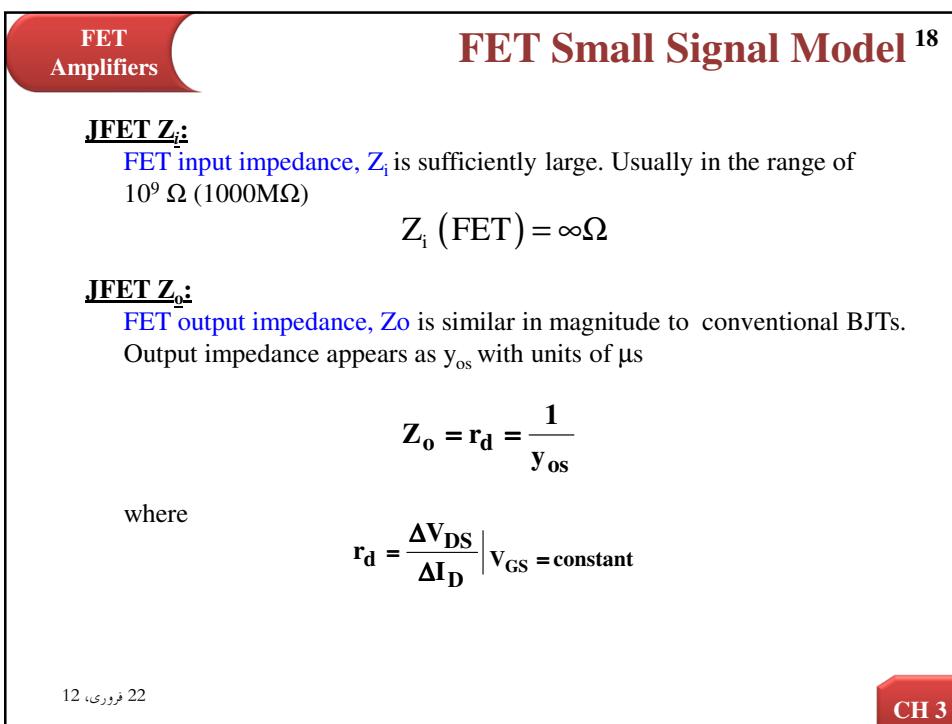
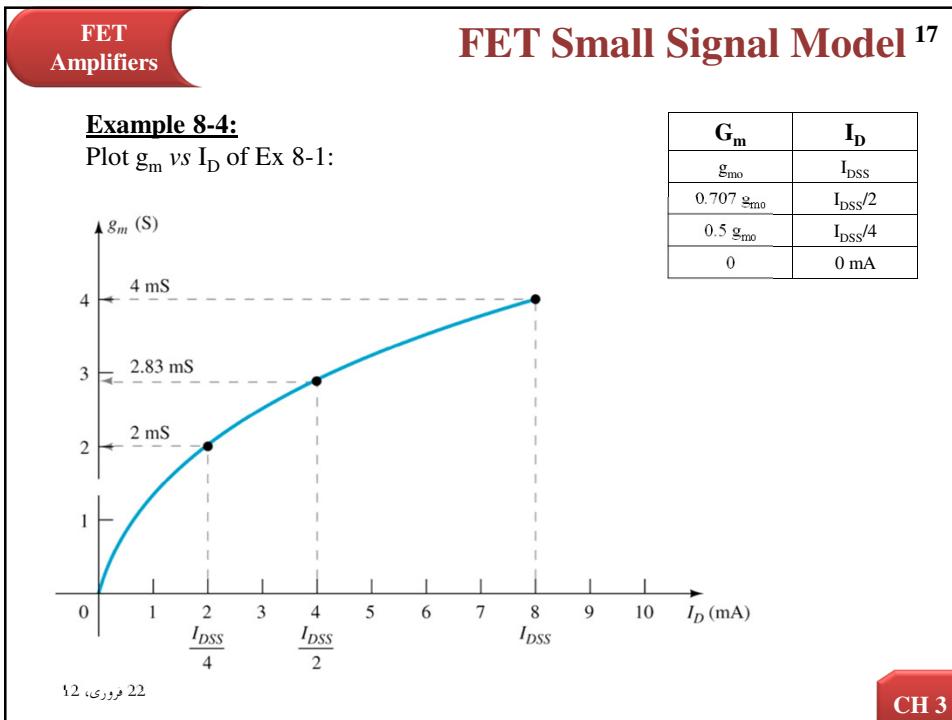
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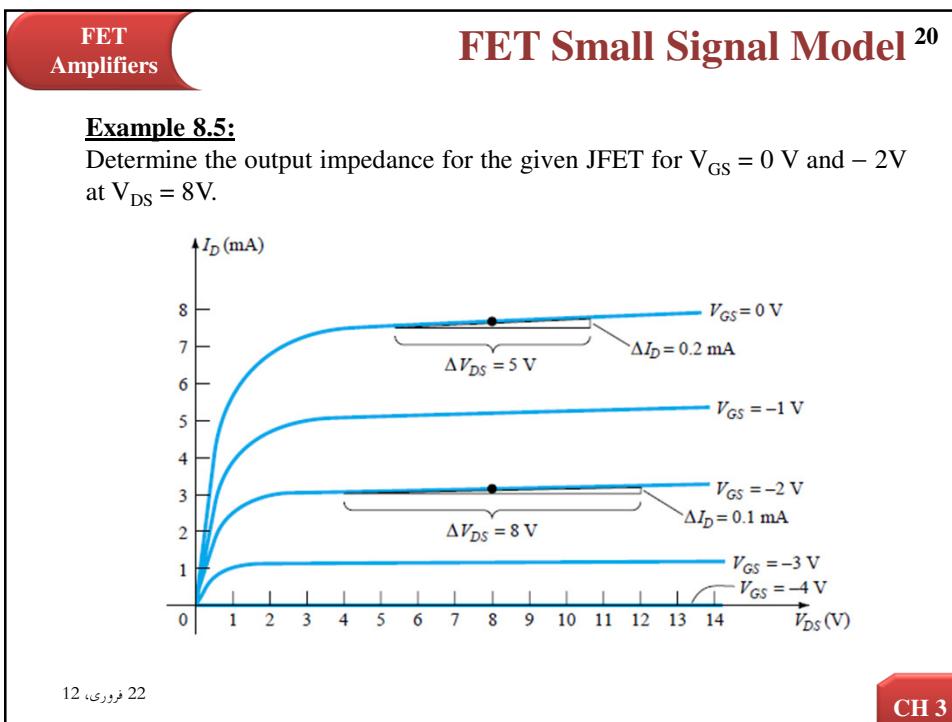
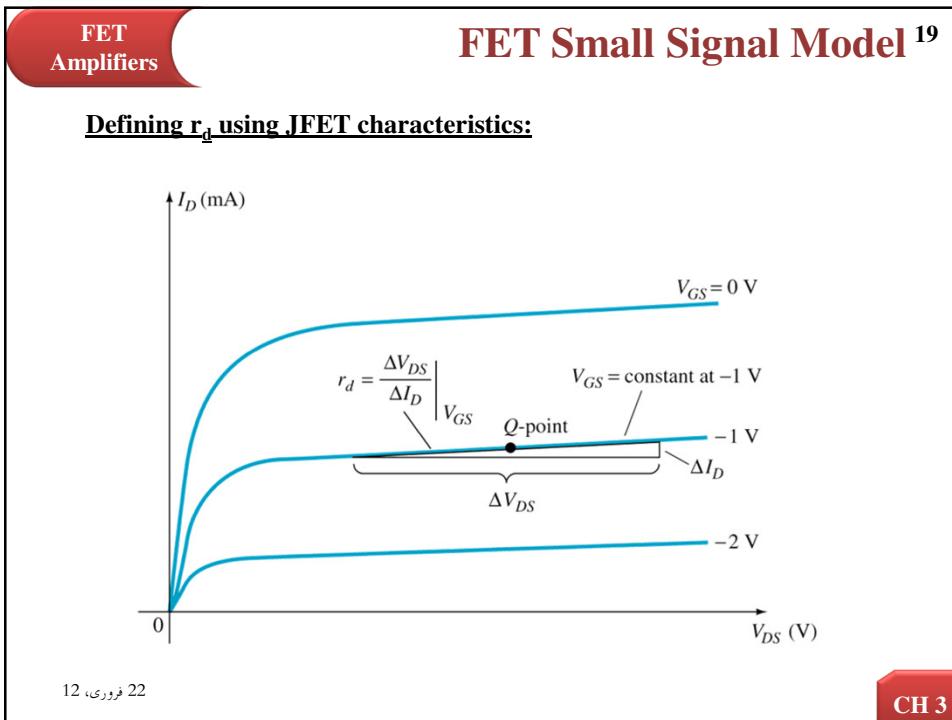
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FET Small Signal Model ¹⁶**Example 8-4:**Plot g_m vs I_D of Ex 8-1:

12، 22

CH 3





FET Amplifiers

FET Small Signal Model ²¹

JFET AC Equivalent:

12. اس. 22

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FET Small Signal Model ²²

Example 8-6:

Given $y_{fs} = 3.8 \text{ mS}$ and $y_{os} = 20 \mu\text{S}$. Sketch the FET ac equivalent model:

12. اس. 22

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JFET Configurations

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JFET Configurations:

1. Fixed bias (Common Source)
2. Self bias
3. Voltage-Divider bias
4. Common Gate
5. Source-Follower (Common Drain)

Important Parameters of AC Analysis:

1. Input impedance
2. Output impedance
3. Voltage Gain

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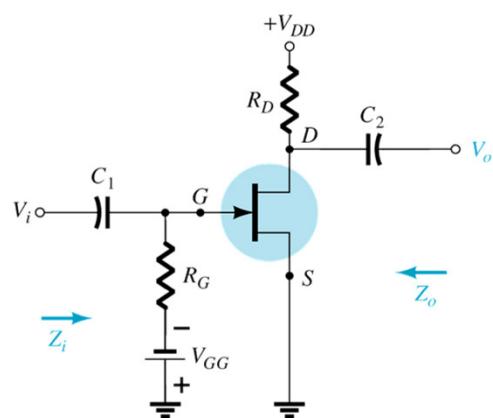
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*Fixed Bias
Configuration*

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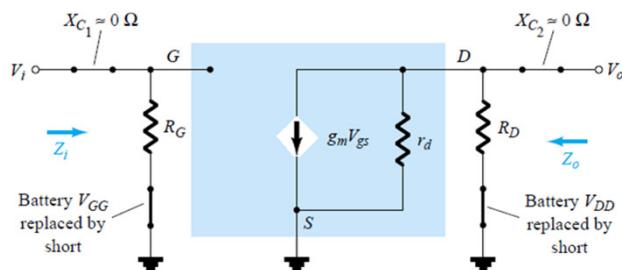
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1. Fixed Bias Configuration (Common Source):



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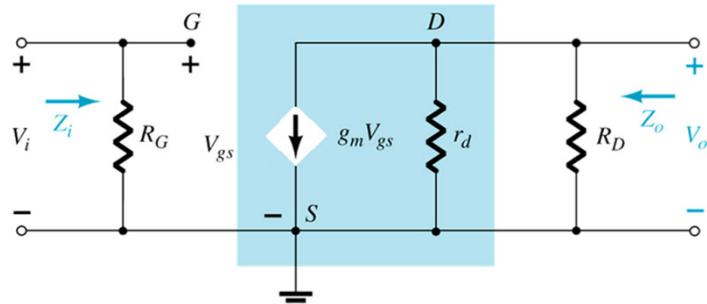
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Determining Z_i :

Substituting the JFET ac equivalent circuit unit into the fixed bias network

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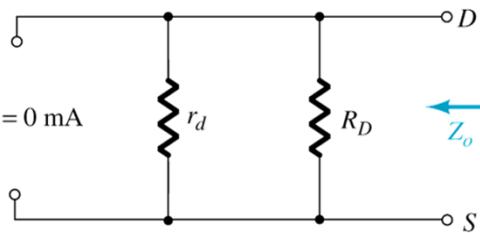
Determining Z_i :

$$Z_i (\text{FET}) = R_G$$

Redrawn network

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Determining Z_o :Set $V_i = 0$ $g_m V_{gs} = 0 \text{ mA}$ 

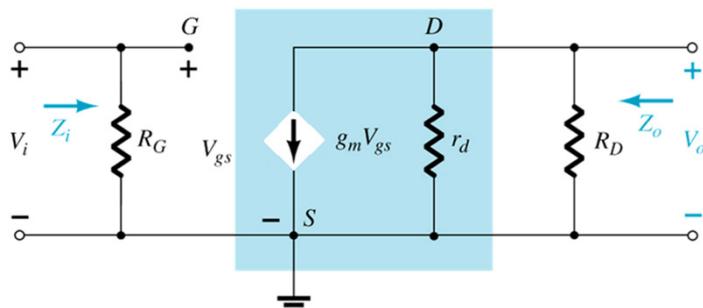
$$Z_o (\text{FET}) = r_d \parallel R_D$$

$$Z_o (\text{FET}) = R_D$$

if $r_d \geq 10R_D$

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Determining A_v :

$$A_v = (V_o / V_i)$$

$$= -g_m (r_d \parallel R_D)$$

$$A_v = (V_o / V_i)$$

$$= -g_m (R_D) \text{ when } r_d \geq 10R_D$$

$$V_o = -g_m V_{gs} (r_d \parallel R_D)$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_i (r_d \parallel R_D)$$

12.1.2.22

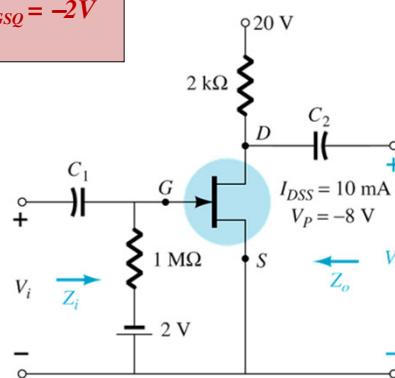
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Example 8-7:

AC analysis of the fixed-bias configuration of Ex 7-1: If $y_{os} = 40 \mu\text{S}$, than, determine:

- a. g_m
- b. r_d
- c. Z_i
- d. Z_o
- e. A_v
- f. A_v (ignoring the effects of r_d)

$$\begin{aligned} I_{DQ} &= 5.625 \text{ mA}; V_{GSQ} = -2 \text{ V} \\ y_{os} &= 40 \mu\text{S} \end{aligned}$$



12.5.22

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***Self Bias
Configuration***

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JFET Self Bias:
Bypassed R_S

12 اس 22

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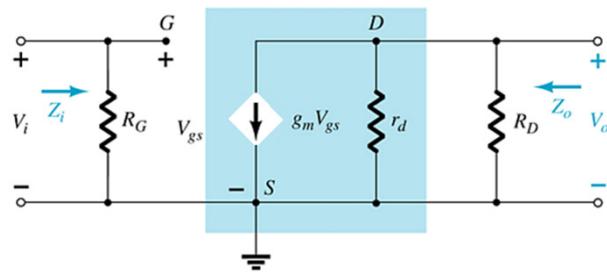
FET Amplifiers

JFET Self Bias:

Fixed bias network following the substitution of the JFET ac equivalent

12 اس 22

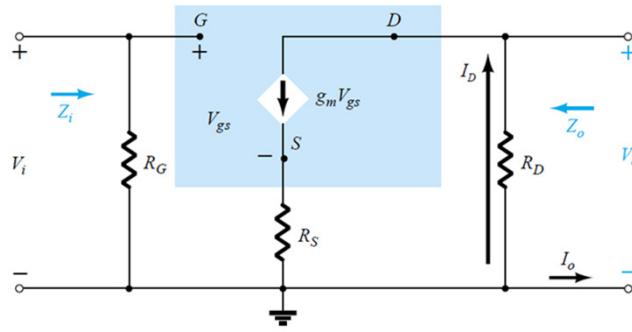
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JFET Self Bias:

Redrawn network

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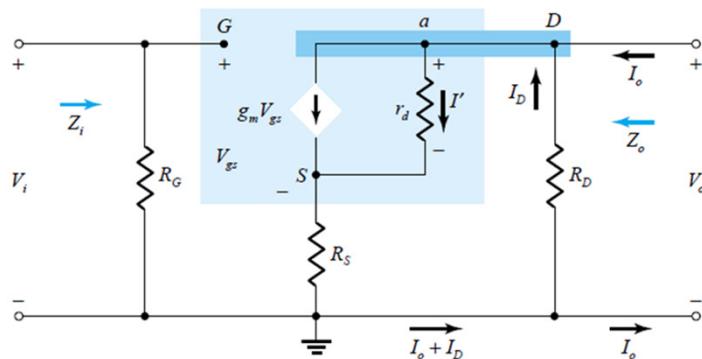
JFET Self Bias:
Unbypassed RS

$$Z_i = R_G$$

$$Z_o = \frac{V_o}{I_o} = R_D$$

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JFET Self Bias:
Unbypassed R_SIncluding the effects of r_d in the self bias JFET configuration

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JFET Self Bias:
Unbypassed R_S

$$Z_o = \frac{\left[1 + g_m R_s + \frac{R_s}{r_d} \right]}{\left[1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d} \right]} R_D$$

$$Z_o \cong R_D$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} \cong -\frac{g_m R_D}{1 + g_m R_s}$$

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FET
Amplifiers

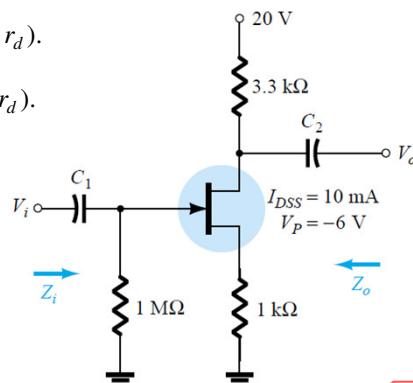
JFET Self Bias 39

Example 8-8:

AC Analysis the self-bias configuration of Ex 7-2:

If $y_{os} = 20 \mu\text{S}$, then, determine:

- g_m
- r_d
- Z_i
- Z_o (with and without the effects of r_d).
Compare the results.
- A_v (with and without the effects of r_d).
Compare the results.



12، ۲۲

CH 3

FET
Amplifiers

JFET Self Bias 40

Computer Analysis:

12، ۲۲

CH 3

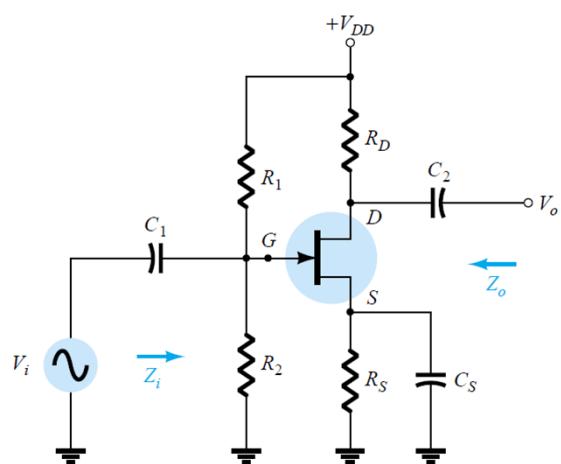
Voltage Divider Configuration

12.1.2.22

CH 3

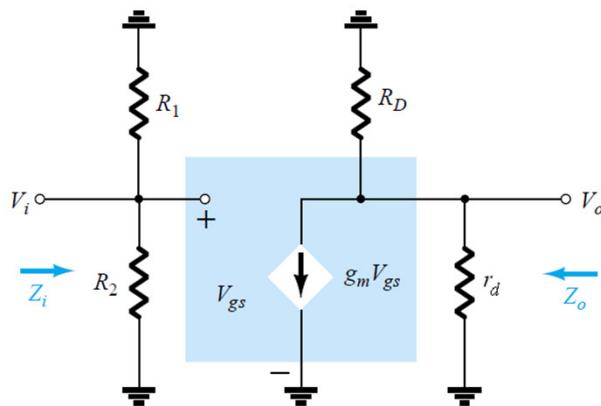
JFET Voltage Divider Bias 42

Voltage Divider Bias:



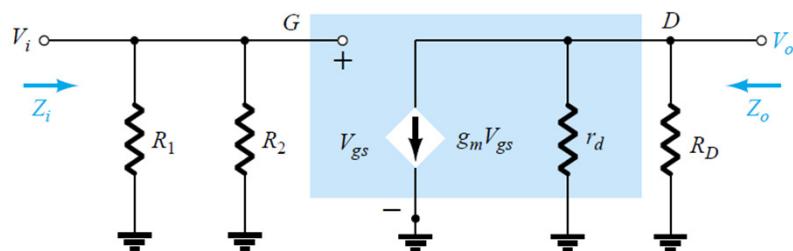
12.1.2.22

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Voltage Divider Bias:

12.1.5.22

CH 3

Voltage Divider Bias:

$$Z_i = R_1 \parallel R_2$$

$$Z_o \cong R_D$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D$$

12.1.5.22

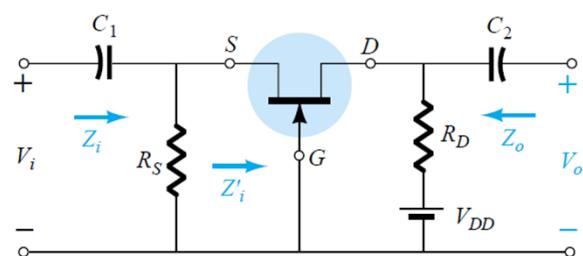
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*Common-Gate
Configuration*

12.1.2.22

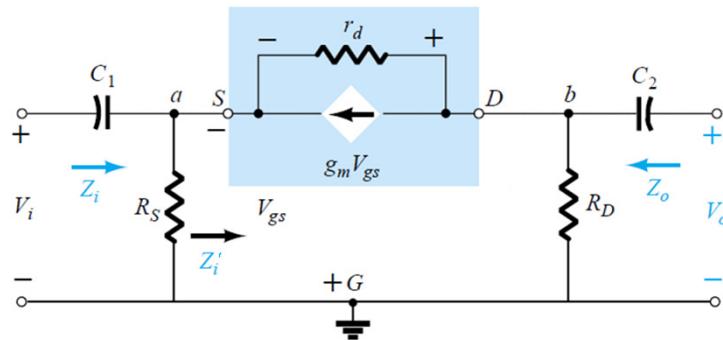
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Common Gate Configuration:



12.1.2.22

CH 3

Common Gate Configuration:

12.5.22

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Common Gate Configuration:

$$Z'_i \equiv \frac{\left[1 + \frac{R_D}{r_d} \right]}{\left[g_m + \frac{1}{r_d} \right]}$$

$$Z_i \equiv R_S \parallel \frac{1}{g_m}$$

$$Z_o \equiv R_D$$

Small-signal equivalent circuit diagram for the JFET common-gate amplifier. It shows the JFET model with transconductance $g_m V_{gs}$, drain resistance r_d , and drain-to-source voltage V_{rs} . The input voltage V' is applied through a source resistor R_S to the gate. The drain current I' is split into two paths: one through the drain resistor R_D to ground, and another through the drain-to-source junction. The output voltage V_o is taken from the drain terminal D .

$$A_v \equiv R_D g_m$$

12.5.22

CH 3

FET
Amplifiers

JFET Common-Gate 49

Example 8-9:

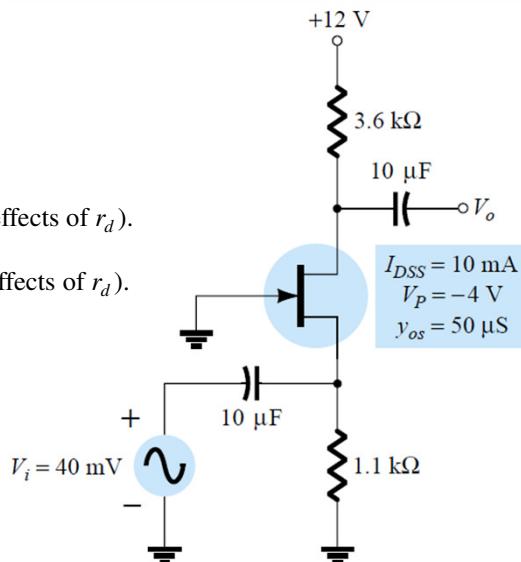
Determine:

- g_m
- r_d
- Z_i
- Z_o (with and without the effects of r_d).

Compare the results.

- V_o (with and without the effects of r_d).

Compare the results.



12.1.22

CH 3

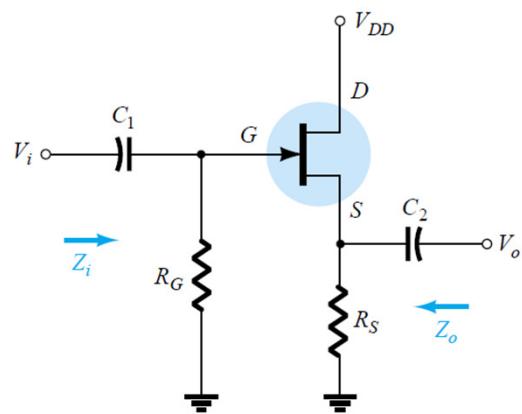
FET
Amplifiers

50

*Source-Follower
(Common-Drain)
Configuration*

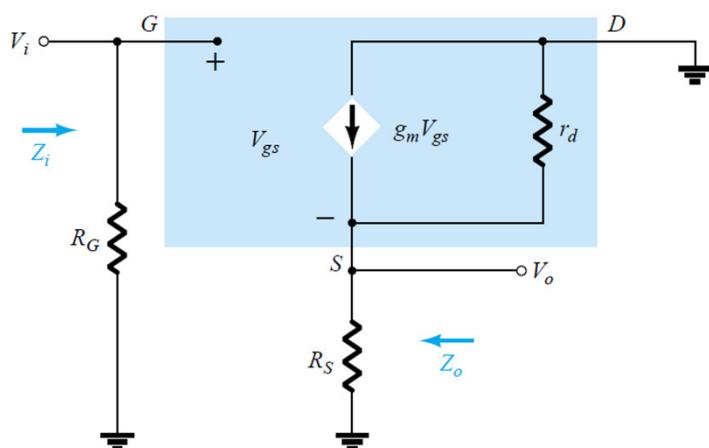
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Source-Follower (CD):

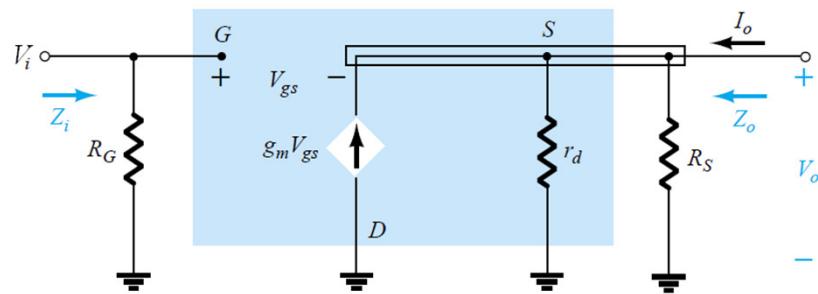
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Source-Follower (CD):

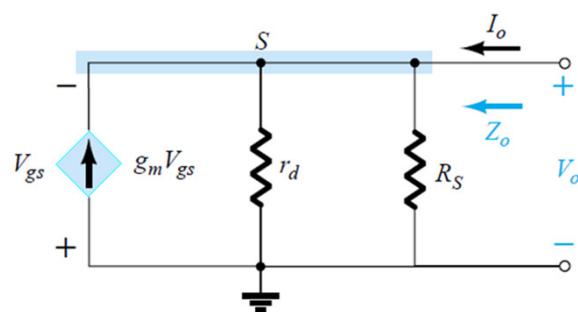
12 . 22

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Common-Follower (CD):

12، ۲۲

CH 3

Common-Follower (CD):Determining Z_o

12، ۲۲

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Common-Follower (CD):

$$Z_i = R_G$$

$$Z_o \cong R_s \parallel \frac{1}{g_m}$$

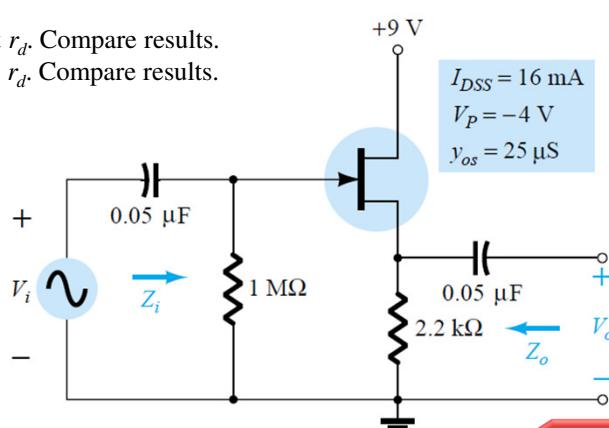
$$A_v \cong \frac{g_m R_s}{1 + g_m R_s}$$

12.1.22

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Example 8-10:AC analysis: $V_{GSQ} = 2.86$ V and $I_{DQ} = 4.56$ mA. Determine:

- a. g_m
- b. R_d
- c. Z_i
- d. Z_o with and without r_d . Compare results.
- e. A_v with and without r_d . Compare results.



12.1.22

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Depletion-Type MOSFETs

MOSFET Configurations 58

MOSFET Configurations:

D-MOSFET:

1. *Voltage Divider*

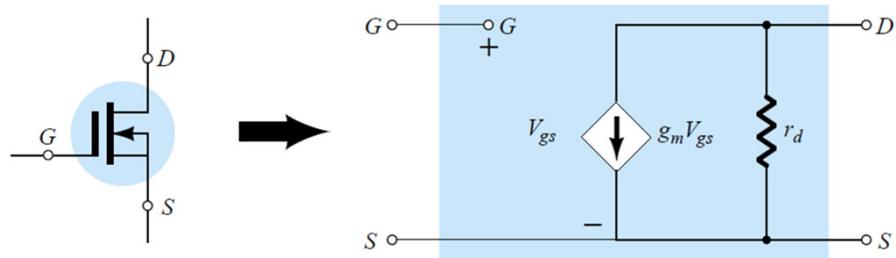
E-MOSFET:

1. *Drain Feedback*
2. *Voltage Divider*

D-MOSFET

12، ۲۲

CH 3

D-MOSFET Configurations ⁶⁰**D-MOSFET Equivalent Model:**

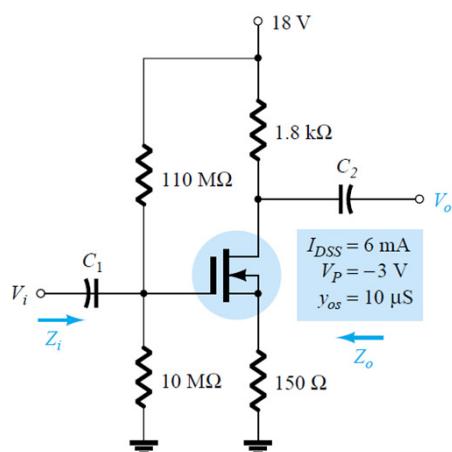
12، ۲۲

CH 3

Example 8-11:

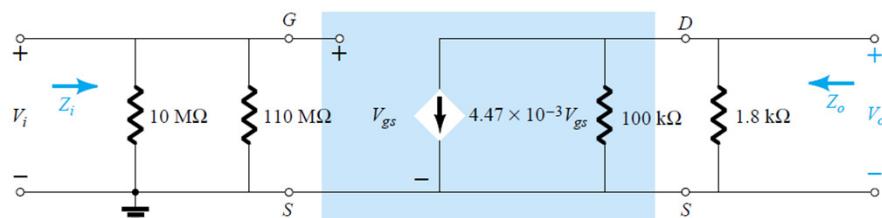
AC analysis (Ex 7-8): $V_{GSQ} = 0.36$ V and $I_{DQ} = 7.6$ mA. Determine:

- g_m and compare to g_{mo} .
- r_d
- Z_i
- Z_o
- A_v
- Sketch the ac equivalent



12، ۲۲

CH 3

Example 8-11:

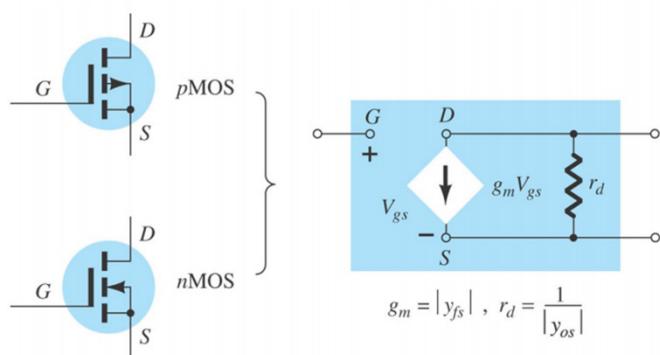
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E-MOSFET

12 . ٢٢

CH 3

E-MOSFET Configurations 64**Equivalent Circuit:**

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})$$

12 . ٢٢

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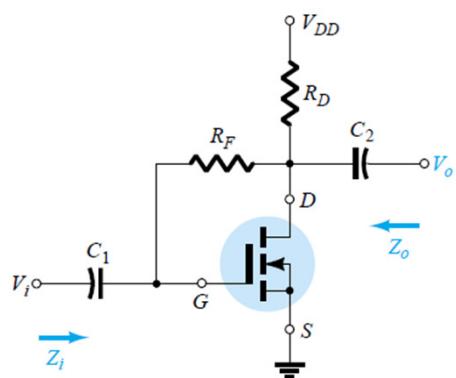
E-MOSFET
Drain-Feedback

12 . ٢٢

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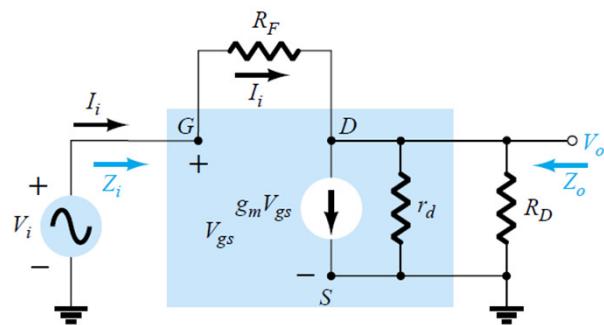
E-MOSFET Configurations ⁶⁶

Drain Feedback:



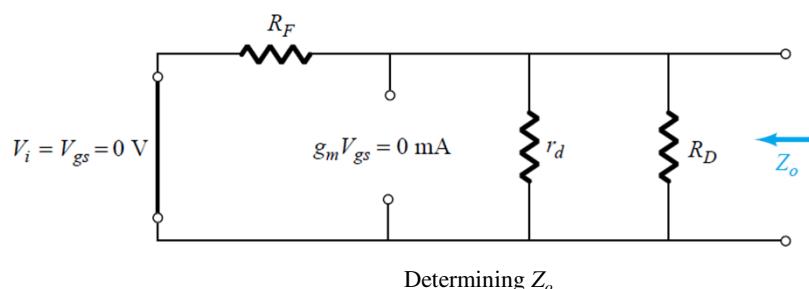
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CH 3

Drain Feedback:

12.1.2.22

CH 3

Drain Feedback:

12.1.2.22

CH 3

Drain Feedback:

$$Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D}$$

$R_F \gg r_d \| R_D, r_d \geq 10 R_D$

$$Z_o = R_F \| r_d \| R_D$$

$$Z_o \cong R_D$$

$R_F \gg r_d \| R_D, r_d \geq 10 R_D$

$$A_v = -g_m(R_F \| r_d \| R_D)$$

$$A_v = -g_m R_D$$

$R_F \gg r_d \| R_D, r_d \geq 10 R_D$

12.15.22

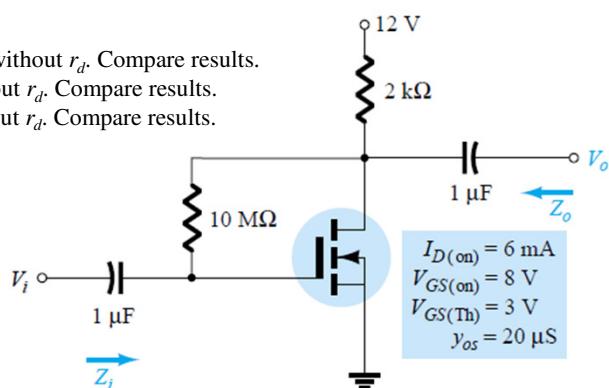
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Example 8-12:

The E-MOSFET of Fig. 8-41 was analyzed in Example 7.11, with the result that $k = 0.24 \times 10^{-3} \text{ A/V}^2$, $V_{GSQ} = 6.4 \text{ V}$, and $I_{DQ} = 2.75 \text{ mA}$.

Determine g_m .

- Find r_d .
- Calculate Z_i with and without r_d . Compare results.
- Find Z_o with and without r_d . Compare results.
- Find A_v with and without r_d . Compare results.



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CH 3

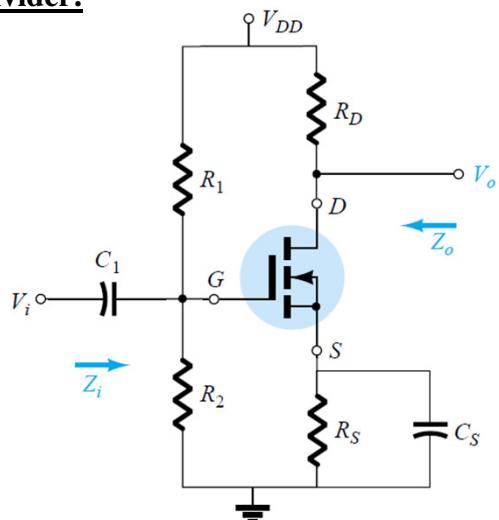
E-MOSFET
Voltage Divider

12.٢٢.٢٢

CH 3

E-MOSFET Configurations 72

Voltage Divider:



12.٢٢.٢٢

CH 3

FET Amplifiers

E-MOSFET Configurations 73

Voltage Divider:

12 اس 22

CH 3

FET Amplifiers

E-MOSFET Configurations 74

Voltage Divider:

$$Z_i = R_1 \parallel R_2$$

$$Z_o = r_d \parallel R_D$$

$$Z_o \cong R_D \quad r_d \geq 10R_D$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_D \parallel R_D)$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad r_d \geq 10R_D$$

12 اس 22

CH 3

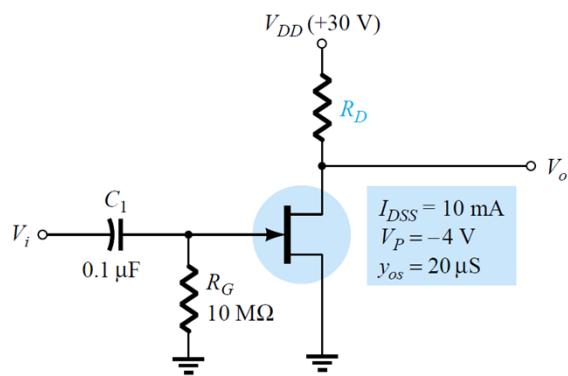
*Designing
FET
Amplifier Network*

12، ۲۲، ۱۲

CH 3

Example 8-13:

Design the fixed-bias network of Fig. 8-44 to have an ac gain of 10.
That is determine the value of R_D .

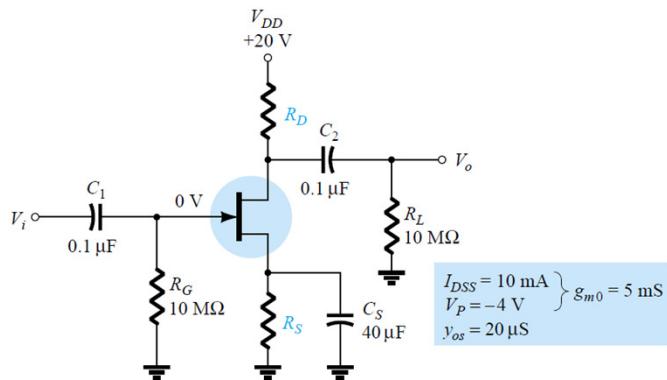


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CH 3

Example 8-14:

With a relatively high level of g_m , select the values of R_D and R_S for the given network, that will result in a gain of 8. For the device $V_{GSQ} = \frac{1}{4} V_P$



12، ۲۲

CH 3

Example 8-15:

With a relatively high level of g_m , select the values of R_D and R_S for the given network, that will result in a gain of 8. For the device $V_{GSQ} = \frac{1}{4} V_P$. Now bypass capacitor has been removed.

12، ۲۲

CH 3

FET Amplifiers

Summary Table 79

TABLE 8.1 Z_i , Z_o , and A_v for various FET configurations

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET]	<p>High (10 MΩ) $= R_G$</p>	<p>Medium (2 kΩ)</p> $= R_D r_d$ $\approx R_D \quad (r_d \geq 10 R_D)$	<p>Medium (-10)</p> $= -g_m(r_d R_D)$ $\approx -g_m R_D \quad (r_d \geq 10 R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET]	<p>High (10 MΩ) $= R_G$</p>	<p>Medium (2 kΩ)</p> $= R_D r_d$ $\approx R_D \quad (r_d \geq 10 R_D)$	<p>Medium (-10)</p> $= -g_m(r_d R_D)$ $\approx -g_m R_D \quad (r_d \geq 10 R_D)$

12.15.22

CH 3

FET Amplifiers

Summary Table 80

Self-bias unbypassed R_S [JFET or D-MOSFET]	<p>High (10 MΩ) $= R_G$</p>	$= \frac{1 + g_m R_S + \frac{R_S}{r_d} R_D}{1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}}$ $= R_D \quad r_d \geq 10 R_D \text{ or } r_d = \infty \Omega$	<p>Low (-2)</p> $= \frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$ $\approx -\frac{g_m R_D}{1 + g_m R_S} \quad [r_d \geq 10(R_d + R_S)]$
Voltage-divider bias [JFET or D-MOSFET]	<p>High (10 MΩ) $= R_1 R_2$</p>	<p>Medium (2 kΩ)</p> $= R_D r_d$ $\approx R_D \quad (r_d \geq 10 R_D)$	<p>Medium (-10)</p> $= -g_m(r_d R_D)$ $\approx -g_m R_D \quad (r_d \geq 10 R_D)$

12.15.22

CH 3

FET Amplifiers

Summary Table 81

Configuration	Z_t	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET]	<p>High ($10 \text{ M}\Omega$) $= [R_G]$</p>	<p>Low ($100 \text{ k}\Omega$) $= [r_d \ R_S \ 1/g_m]$ $\approx [R_S \ 1/g_m] \quad (r_d \gg 10 R_S)$</p>	<p>Low (< 1) $= \frac{g_m(r_d \ R_S)}{1 + g_m(r_d \ R_S)}$ $\approx \frac{g_m R_S}{1 + g_m R_S} \quad (r_d \gg 10 R_S)$</p>
Common-gate [JFET or D-MOSFET]	<p>Low ($1 \text{ k}\Omega$) $= [R_S \ \frac{r_d + R_D}{1 + g_m r_d}]$ $\approx [R_S \ \frac{1}{g_m}] \quad (r_d \gg 10 R_S)$</p>	<p>Medium ($2 \text{ k}\Omega$) $= [R_D \ r_d]$ $\approx [R_D] \quad (r_d \gg 10 R_D)$</p>	<p>Medium ($+10$) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\approx [g_m R_D] \quad (r_d \gg 10 R_D)$</p>

12.15.22

CH 3

FET Amplifiers

Summary Table 82

Drain-feedback bias E-MOSFET	<p>Medium ($1 \text{ M}\Omega$) $= [\frac{R_F + r_d \ R_D}{1 + g_m(r_d \ R_D)}]$ $\approx [\frac{R_F}{1 + g_m R_D}] \quad (r_d \gg 10 R_D)$</p>	<p>Medium ($2 \text{ k}\Omega$) $= [R_F \ r_d \ R_D]$ $\approx [R_D] \quad (R_F, r_d \gg 10 R_D)$</p>	<p>Medium (-10) $= [-g_m(R_F \ r_d \ R_D)]$ $\approx [-g_m R_D] \quad (R_F, r_d \gg 10 R_D)$</p>
Voltage-divider bias E-MOSFET	<p>Medium ($1 \text{ M}\Omega$) $= [R_1 \ R_2]$</p>	<p>Medium ($2 \text{ k}\Omega$) $= [R_D \ r_d]$ $\approx [R_D] \quad (R_d \geq 10 R_D)$</p>	<p>Medium (-10) $= [-g_m(r_d \ R_D)]$ $\approx [-g_m R_D] \quad (R_d \geq 10 R_D)$</p>

12.15.22

CH 3

*Effect of
 R_L and R_{sig}*

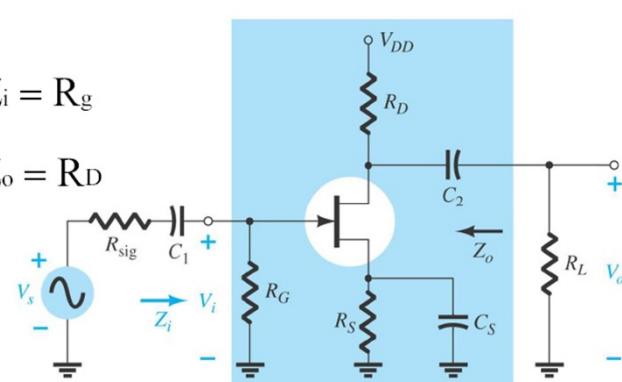
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CH 3

Effect of R_L and R_{sig} :

$$Z_i = R_g$$

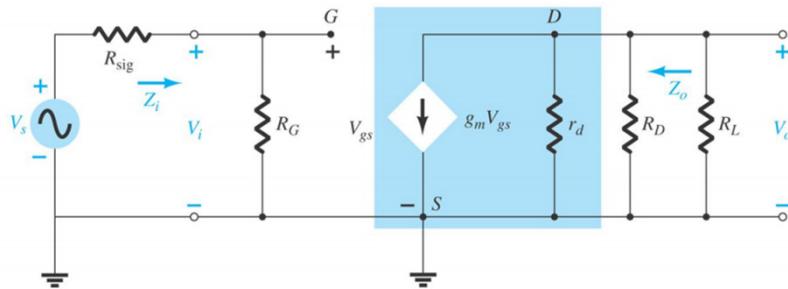
$$Z_o = R_D$$



$$A_v = \left[\frac{V_o}{V_i} \right] = -g_m (r_d // R_D // R_L)$$

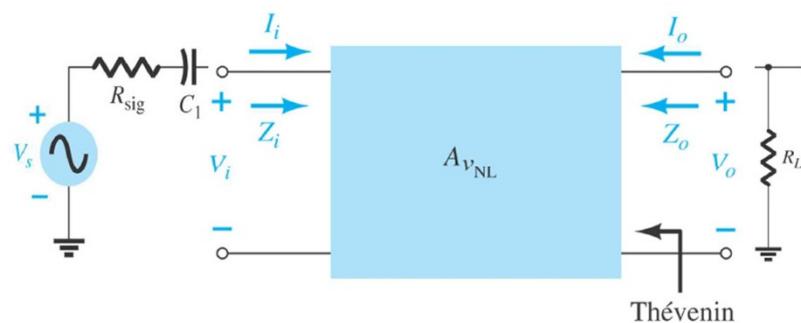
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Effect of R_L and R_{sig} :

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CH 3

Effect of R_L and R_{sig} :

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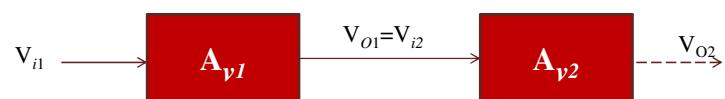
CH 3

*Cascade
Configuration*

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CH 3

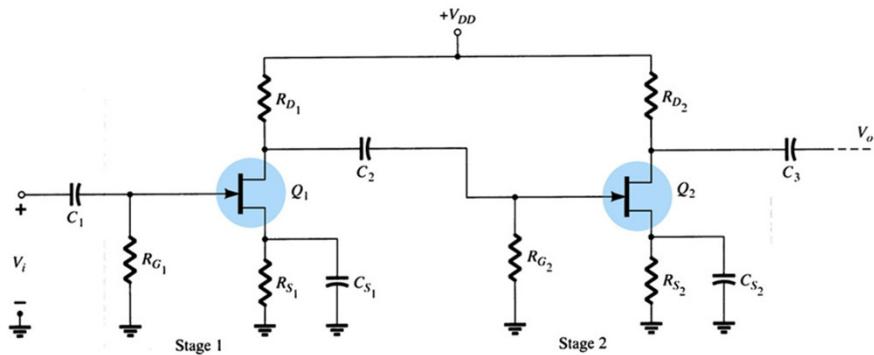
Cascade Configuration:



$$A_v = A_{v1} A_{v2} \dots$$

12، ۲۲

CH 3

Cascade Configuration:

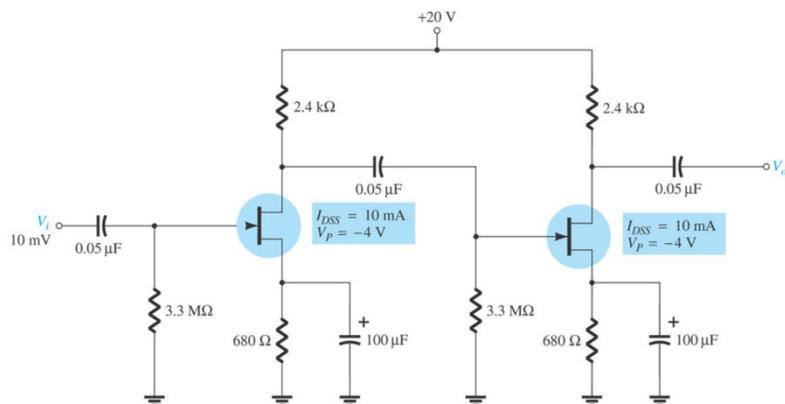
$$A_v = A_{v1}A_{v2} = g_m g_m R_{D1} R_{D2}$$

12 . 5, 22

CH 3

Example 8-16:

Calculate the dc bias, voltage gain, input impedance, output impedance and resulting output voltage for the cascade amplifier shown in Fig. 8.49. Calculate the load voltage if a 10-k load is connected across the output.

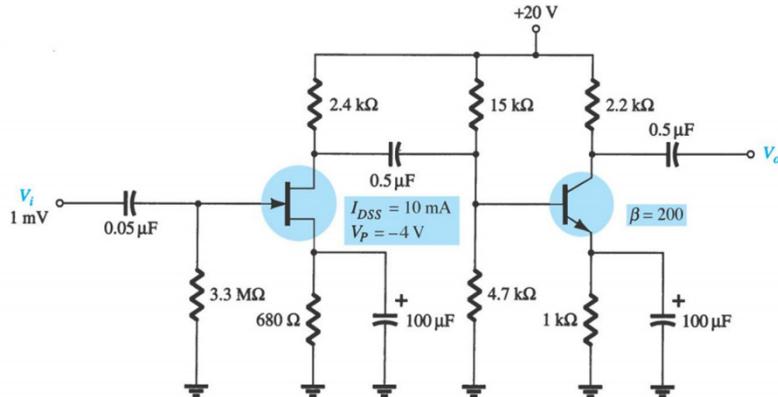


12 . 5, 22

CH 3

Example 8-17:

For the cascade amplifier of Fig. 8-50, use the dc bias calculated in Example 8-15 and 8-16 to calculate the input impedance, output impedance, voltage gain, and resulting output voltage.



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CH 3

*Practical
Applications*

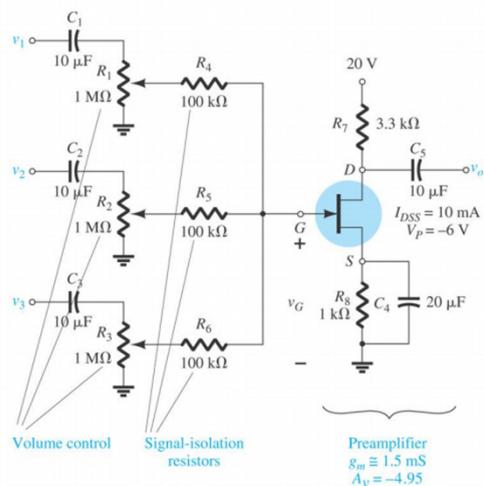
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CH 3

FET Amplifiers

Practical Applications 93

1. Three channel audio mixer



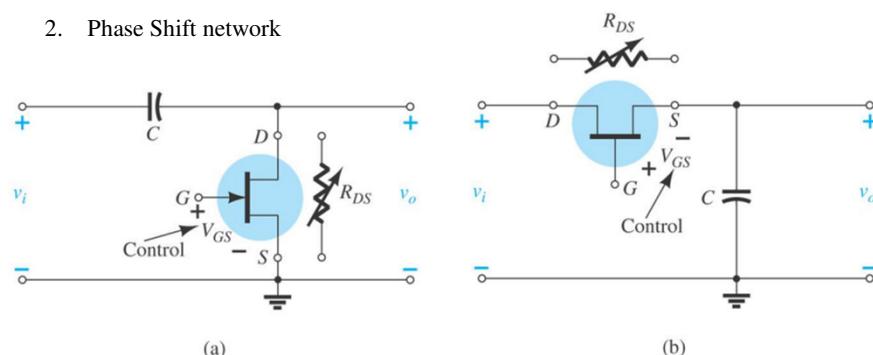
12 اسے 22

CH 3

FET Amplifiers

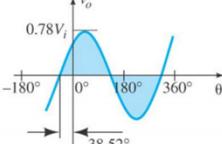
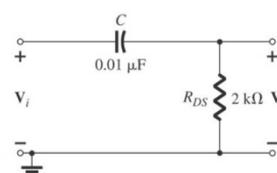
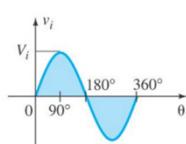
Practical Applications 94

2. Phase Shift network



(a)

(b)



12 اسے 22

CH 3

**FET
Amplifiers**

Home Task 95

Reading:

1. Summary
2. Equations
3. Computer analysis

Problems:

1. Sec 8.2: (odd)
2. Sec 8.3: 17,18
3. Sec 8.4: 19,21
4. Sec 8.5:23,25
5. Sec 8.6: 27,29
6. Sec 8.7: 31
7. Sec 8.8: 33,35,37
8. Sec 8.10: 39,41
9. Sec 8.11: 43
10. Sec 8.12: 45
11. Sec 8.14: 47
12. Sec 8.15: 49

12 درس 22

CH 3

**FET
Amplifiers**

References 96

1. Bolestad
2. Paynter

12 درس 22

CH 3